Analytic Expressions for the Optimum Source & Load Impedance and Associated Large-Signal Gain of an RF Power Transistor

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Abstract — **This paper presents for the first time analytic expressions for the optimum source and load impedance and associated large-signal gain for a transistor with series inductive and parallel capacitive feedback in addition to input and output capacitance. Both class A and B are considered. The computed results are shown to be in good agreement with experimental data.**

I. INTRODUCTION

The determination of the optimum source and load impedance at microwave frequencies for a transistor to deliver its maximum output power (or best linearity or lowest noise figure) is now normally undertaken using automatic load-pull test equipment. However, such equipment does not exist at HF, VHF and UHF frequencies. In fact, these frequencies present a number of challenges for automatic load-pull test equipment since at HF the line length in air is 10m, the supply voltage for the transistor may be as high as 900V implying a peak RF voltage of 1800V, the power level can be up to 1KW, and the transistor may be push-pull rather than single-ended. The normal procedure for the experimental determination of optimum source and load impedances for maximum power output at these frequencies is to construct and then empirically adjust a narrow-band amplifier circuit until the maximum power is obtained. The transistor is next removed and the impedance seen by the device is then measured using a vector network analyser. For push-pull devices a decision has to be made at this stage as to whether to measure terminal-to-terminal or terminal-to-ground - both situations create their own problems. Terminal-to-ground measurements require that the terminal not being measured is terminated with an impedance identical to that which the transistor presents to the circuit in the off half-cycle, while terminal-to-terminal measurements require the use of baluns and balanced calibration standards. Even for single-ended transistors the procedure is subject to several errors e.g. one is never sure that the 'optimum' load impedance has in fact been presented to the transistor, the effect of the impedance at harmonics on the measured output power is usually ignored, and it is difficult to measure accurately an impedance that can be <1Ω. Thus although RF power transistor manufacturers quote values for the optimum source and load impedance of the transistor on their data sheets, these values are in fact only approximate.

In this paper analytic expressions are presented for the first time for the optimum source and load impedance and associated large-signal gain in class A or B of an RF power transistor that may have series inductive and/or parallel capacitive feedback in addition to input and output capacitance. This paper is an extension of the technique attributed to Cripps [1]. It will also be shown how the effect of the package on the calculated value can easily be accounted for. It will be shown that the calculated results are in good agreement with published data bearing in mind the inaccuracies associated with both methods. This theory can be used as a check on the experimentally measured value or as a means of avoiding having to make a different jig for every frequency and device of interest.

II. THEORETICAL ANALYSIS

Cripps [1] assumed an ideal transistor that consists of just a voltage-controlled current generator as shown in Fig. 1.

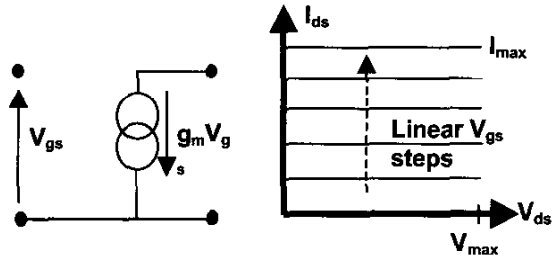

Fig. 1. Ideal Transistor

In class A the bias point is $V_{ds}=V_{max}/2$, $I_{ds}=I_{max}/2$. To obtain the maximum linear power output from such a device the RF voltage and current must have amplitudes of $V_{max}/2$ and $I_{max}/2$, respectively, resulting in a maximum linear RF output power of $V_{max}I_{max}/8$. To obtain an RF voltage and current swing of $V_{max}/2$ and $I_{max}/2$ the load impedance must be

$$R_{opt} = \frac{V_{\max}}{I_{\max}} \tag{1}$$

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If the input voltage is increased beyond the value required to create a current swing of $\pm I_{max}/2$, then the current waveform will be clipped. This will result in higher power output but gain compression will occur and distortion will be generated. It can be shown [2] that (1) is also the optimum load impedance for pure class B operation. In this paper the Cripps analysis is extended to a transistor having input, output and feedback capacitance as well as series inductive common-lead feedback as shown in Fig. 2. This model of a transistor is applicable to most RF and microwave field effect transistors including GaAs FETs, PHEMTs and Si LDMOS and VDMOS transistors.

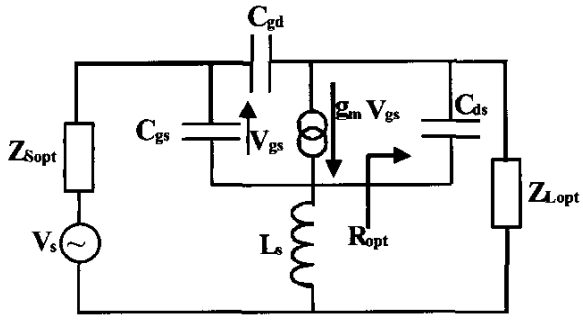

Fig. 2. Transistor with feedback

The key fact to remember in deriving an expression for Z_{Lopt} is that when the amplitude of V_{gs} is such that the drain current amplitude reaches $I_{max}/2$, then the current generator must see a load impedance of R_{opt} in order for it to deliver its maximum linear output power. In this circumstance circuit analysis shows that Z_{Lopt} is given by

$$Z_{Lopt} = \frac{R_{opt} - \omega^2 L_S (R_{opt} C_{ds} - C_{gs}/g_m) - j\omega L_S}{1 - j\omega[C_{gd}/g_m + R_{opt}(C_{gd} + C_{ds})]} \quad (2)$$

This is an exact equation based on the model in Fig. 2. For class A operation $g_m = g_{mDC}$ where g_{mDC} is the DC value of g_m as published in the manufacturer's data sheet, but for class B operation $g_m = g_{mDC}/2$ since the output current is a half-sinusoid for which the amplitude of the fundamental component is half the peak value of the half-sinusoid [2].

For a power amplifier the source impedance is normally chosen to maximize the gain when the load impedance is Z_{Lopt}, in which case the optimum source impedance is the complex conjugate of the input impedance. Elementary circuit analysis shows that Z_{Sopt} is given exactly by

$$Z_{Sopt} = \frac{L_S g_m}{C_{gs} + C_{gd}(1 + g_m R_{opt})} + j\frac{1 - \omega^2 L_S C_{gs} + \omega^2 L_S C_{ds} g_m R_{opt}}{\omega(C_{gs} + C_{gd}(1 + g_m R_{opt})} \quad (3)$$

Z_{Sopt} is often calculated using the S parameters of the FET when terminated in a load Z_{Lopt}. This method will not normally give an accurate answer for large-signal class B or A/B operation since the S parameters are usually measured under small-signal RF operation around a class A/B bias point. Consequently, the S parameters are measured with the transistor conducting throughout the RF cycle, in other words the S parameters are measured using the class A value for g_m which is twice the value that will be achieved under large-signal class B or A/B operation.

Finally, the gain G of the transistor when terminated in Z_{Sopt} and Z_{Lopt} is given exactly by

$$G = \frac{g_m^2 R_{opt}}{\mathrm{Re}(Z_{Sopt}) * \omega(C_{gs} + C_{gd}(1 + g_m R_{opt}))} \quad (4)$$

III. IMPLICATIONS OF PRECEDING ANALYSIS

A number of conclusions can be reached from the preceding analysis:

1. It can be shown that the real part of Z_{Lopt} is given approximately by

$$\mathrm{Re}(Z_{Lopt}) \approx \frac{R_{opt}(1 + \omega^2 L_s C_{gd}) + \omega^2 L_s C_{iss}/g_m}{1 + \omega^2 R_{opt}^2 C_{oss}^2} \quad (5)$$

where $C_{iss} = {}_{gs} + C_{gd}$ and $C_{oss} = {}_{ds} + C_{gd}$. At low frequencies such that $1 >> (\omega R_{opt} C_{oss})^2$, then $Re(Z_{Lopt}) \approx R_{opt}$. However, at high frequencies where the inequality does not hold, then $Re(Z_{Lopt}) \approx 1/R_{opt}$. This has important consequences. At low frequencies it is advantageous to use a high voltage transistor (e.g. 50V supply voltage) since this increases R_{opt} and hence $Re(Z_{Lopt})$ which makes broadband matching easier. However, at high frequencies it is counter-productive to use a high voltage transistor since a net decrease in the value of $Re(Z_{Lopt})$ would occur unless C_{oss} decreases by more than R_{opt} increases. This is undoubtedly one reason why no 50V MOSFETs are commercially available at 1GHz and above.

2. In a well-designed transistor neither L_S nor C_{gd} has a major effect on $Re(Z_{Lopt})$, C_{oss} is the dominant term that causes $Re(Z_{Lopt})$ to be less than R_{opt}.

3. Although L_S and C_{gd} have little effect on Z_{Lopt} these elements have a first order effect on Z_{Sopt}, in fact $Re(Z_{Sopt})$ is zero if $L_S = 0$. One of the advantages of LDMOS compared to VDMOS is higher gain as a result of reduced source inductance but, as (3) shows, this is accomplished with a lower value [3] for $Re(Z_{Sopt})$ which makes broadband impedance matching more difficult. As an example, Semelab VDMOS part D2012UK and Motorola

LDMOS part MRF6522 are both rated as 10W parts at 1GHz. Both parts use similar packages but whereas the D2012UK has a published $Re(Z_{Sopt})$= 5Ω, the LDMOS part has $Re(Z_{Sopt})$= 2Ω.

4. It is well known (see, for example [2]) that a given transistor will have 6dB less gain in Class B than in Class A if the source and load impedance remain the same. This can be deduced from (4) due to the square-law dependence of G on g_m and, as previously noted, g_m is halved for Class B operation. However, in practice the gain reduction is less than 6dB, typically around 3dB. Equations (2) and (3) taken together provide the explanation for this improvement since $Re(Z_{Sopt})$ is also directly proportional to g_m resulting in G having only a linear dependence on g_m. The fact that the optimum source impedance changes from Class A to Class B appears to have been overlooked in previous publications. An additional factor that also helps reduce the 6dB gain reduction to a small extent is that the transistor is usually used in Class A/B rather than in pure Class B so as to avoid the gain expansion that occurs at low output power as a consequence of the soft turn-on characteristic.

IV. EFFECT OF THE PACKAGE

It is assumed in this paper that the effect of the package can be adequately accounted for by inserting a lossless 2-port network before and after the transistor die as shown in Figure 3.

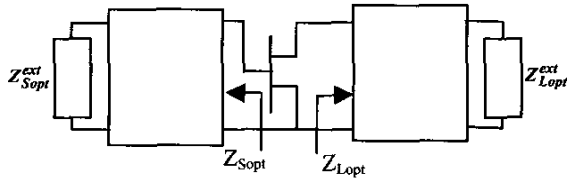

Fig. 3. Effect of package on optimum source and load impedances.

In this situation the optimum load impedance at the terminals of the package is given by

$$Z^{ext}_{Lopt} = \frac{B - Z_{Lopt} D}{Z_{Lopt} C - A} \qquad (6)$$

with a similar expression for the external optimum source impedance. It is the external values that are published in manufacturers' data sheets and it is these values that are quoted in the examples below.

V. APPLICABILITY AND LIMITATIONS OF THE ANALYSIS

Strictly speaking, equations (2)-(4) are only valid for pure class A or B operation. However, detailed analysis [4] shows that the typical deep class A/B bias - whereby the quiescent current is no more than 10% of the peak RF current - results in g_m being underestimated by at most 6% if the class B value for g_m is used instead.

This analysis ignores any effects resulting from the soft current turn-on and saturation characteristics. The latter effect blurs the point at which the device passes from being linear, and this makes experimental verification more difficult.

The finite on-resistance or knee voltage associated with a transistor means that the RF voltage cannot swing down to 0V. Expressed another way, the RF voltage swing is less than half the DC drain voltage. R_{opt} needs to be reduced below the value given in (1) to account for this effect (see, for example, [2]). The analysis also ignores the voltage dependence of any of the capacitances.

Finally, at HF, VHF and UHF frequencies it is very common to use push-pull operation with each half of the device biased in class B or A/B. Each half of the transistor needs to see an impedance to ground identical to that given by (2). However, the data sheets for push-pull transistors from many manufacturers specify the optimum load impedance terminal-to-terminal rather than terminal-to-ground. This assumes that the terminal-to-terminal impedance is twice the terminal-to-ground value.

VI. EXAMPLES

The Semelab D1017UK, Motorola MRF141 and Philips BLF147 Si RF power MOSFETs are all designed to deliver 150W at 175MHz. These transistors all use the same package. The exact value of source and gate inductance for the Motorola and Philips parts is not published but it is assumed to be the same as for the Semelab part. Even if it is higher, the frequency is sufficiently low that its effect is relatively insignificant. All devices are assumed to have the same on-resistance or knee voltage such that the maximum drain voltage swing is ±23V and, hence, the same value of R_{opt}=1.76Ω. Table 1 lists the calculated and published Z_{Lopt} , Z_{Sopt} and RF gain for these parts. It can be seen that there is good agreement between the measured and calculated results considering the inaccuracies associated with both the calculated and published data.

TABLE 1
CALCULATED vs PUBLISHED DATA

	D1017UK	BLF147	MRF141
Calculated Z_{Sopt}	3.1 + j2.5	1.8 + j1.1	2.5 + j2.3
Published Z_{Sopt}	4.0 + j4.4	1.5 + j0.5	1.0 + j0.2
Calculated Z_{Lopt}	1.7 - j1.7	1.2 – j1.3	1.1 – j1.3
Published Z_{Lopt}	2.2 - j7.1	1.0 - j0.5	1.5 + j0.0
Calculated RF Gain	14.5	12.2	13.5
Published RF Gain	14	10	10

The Motorola MRF6522 and MRF282 are LDMOS devices rated at 10W at 1GHz and 2GHz, respectively. For these two devices the model in Fig. 2 was first fitted to the published *S* parameters. The only unknown parameters in the model are the source, gate and drain inductances, all other parameters were taken from the manufacturer's data sheet and the mechanical dimensions of the package. The optimum source and load impedance and associated large-signal gain were then calculated from (2)-(4). Table 2 shows a comparison between the published and calculated values. Once again, reasonable agreement is obtained considering the inherent errors associated with both calculated and published data. While it would be nice to do a comparison for higher power LDMOS transistors, these invariably incorporate internal impedance matching at the output and/or input but the details of the matching network are not disclosed in data sheets. An accurate comparison is not possible for these devices without access to this information.

TABLE 2
CALCULATED vs PUBLISHED DATA

	MRF6522 @ 1GHz	MRF282 @2GHz
Calculated Z_{Sopt}	0.93 + j3.6	1.8 + j1.1
Published Z_{Sopt}	2.0 + j1.0	1.9 - j1.6
Calculated Z_{Lopt}	7.1 + j8.6	3.6 + j4.2
Published Z_{Lopt}	6.5 + j3.0	3.6 - j0.2
Calculated RF Gain	17.3	13.7
Published RF Gain	17	11.5

VII. CONCLUSIONS

This paper has presented for the first time analytic expressions for the optimum source and load impedance and associated large-signal gain for a transistor with series inductive and parallel capacitive feedback in addition to input and output capacitance. Both class A and B were considered. It has been shown that the output capacitance is the dominant factor responsible for the reduction in the value of $Re(Z_{Lopt})$ from its intrinsic value and that feedback has relatively little effect. However, series inductive and parallel capacitive feedback have a first order effect in determining the value of Z_{Sopt}.. The computed results were shown to be in good agreement with experimental data.

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